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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOLE, TIMOTHY J	
ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,908	RODEN ET AL.	
	Examiner	Art Unit	
	Timothy J. Dole	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: (10) in paragraph [0013], line 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugishima et al.

Referring to claim 1, Sugishima et al. discloses an AC ground fault detector system (fig. 3) for sensing an AC signal indicative of an unintended electrical path between a load (fig. 3 (9)) driven by a power source (fig. 3 (1)) and a reference potential (fig. 3), said system comprising: a first power conductor (fig. 3 (+)) coupled to a first terminal of said power source (fig. 3); a second power conductor (fig. 3 (-)) coupled to a second terminal of said power source (fig. 3); a switching mechanism (fig. 3 (4g-4l)) coupled to the first and second power conductors and operative for alternately connecting a phase of said load with the first and second power conductors according to a predetermined switching rate (column 1, lines 51-56), whereby, during normal operation, voltages developed at the first power conductor and second power conductor are substantially constant with respect to a reference (column 1, lines 13-16); and whereby, in the event of an occurrence of said unintended electrical path of at least one phase of the load with the reference potential, time varying voltages are developed at the first power conductor and second power conductor associated with the switching rate (column

6, lines 34-39); a detector (fig. 3) comprising an input port coupled to the first power conductor for receiving the voltage or current signal on the first power conductor (fig. 3); a processing circuit (fig. 3 (24p)) for processing the received signal and comparing with a threshold value; and an output port (fig. 3 (23)) for generating an output signal based on said comparison; whereby the occurrence of the unintended electrical path between the load and reference potential causes a change in the voltage or current signal on the first power conductor of sufficient magnitude relative to the threshold value for detection by said detector such that the output signal of the detector is indicative of a detected fault (column 5, lines 9-41).

Referring to claim 2, Sugishima et al. discloses the system as claimed, further comprising a controller (fig. 5) responsive to the output signal for interrupting power between the load and the first and second power conductors when the output signal is indicative of a detected fault (column 4, lines 27-66).

Referring to claim 3, Sugishima et al. discloses the system as claimed wherein the power interruption occurs via switch openings within the switching mechanism (column 4, lines 27-66).

Referring to claim 9, Sugishima et al. discloses the system as claimed wherein said load comprises a multi-phase motor (fig. 3 (9) and column 5, lines 17-19).

Referring to claim 10, Sugishima et al. discloses the system as claimed wherein said switching mechanism includes pairs of switches (fig. 3 (4g and 4j), (4h and 4k) and (4i and 4l)), each said pair of switches having a common terminal coupled to a respective phase of said multi-phase motor, and wherein for each of said pairs of switches, a first

switch of said pair is operative for selectively coupling the first power conductor to the respective phase of said multi-phase motor, and a second switch of said pair of switches is operative for selectively coupling the second power conductor to the respective phase of said multiphase motor (fig. 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 5, 7, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Konrad et al.

Referring to claims 4 and 17, Sugishima et al. discloses the system as claimed except wherein the processing circuit comprises a filter responsive to the received voltage or current signal on the first power conductor signal for providing a filtered signal component relative to the reference potential; and a comparator responsive to the filtered signal component for comparing with said threshold value for providing said output signal.

Konrad et al. discloses a ground fault detector for an AC motor wherein the processing circuit comprises a filter (column 3, lines 26-29) responsive to the received voltage or current signal on the first power conductor signal for providing a filtered signal component relative to the reference potential; and a comparator (fig. 2 (90)) responsive to

the filtered signal component for comparing with said threshold value for providing said output signal.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the filter of Konrad et al. into the system of Sugishima et al. for the purpose of preventing incorrect data from being processed whereby increasing the accuracy of detecting faults (column 3, lines 26-29).

Referring to claim 5, Sugishima et al. discloses the system as claimed except wherein said filter comprises a capacitor coupled to a resistor network.

Konrad et al. discloses the filter comprises a capacitor coupled to a resistor network (column 3, lines 26-29).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the filter of Konrad et al. into the system of Sugishima et al. for the same purpose as given in claim 4, above.

Referring to claim 7, Sugishima et al. discloses the system as claimed except for an impedance network having a first input port coupled to one of the first and second power conductors and a second input port coupled to the reference potential, the other of the first and second power conductors coupled directly to the reference potential, the impedance network having coupled between the first and second input ports at least one of a resistive or inductive load.

Konrad et al. discloses an impedance network (fig. 2) having a first input port (fig. 2 cathode of (98)) coupled to one of the first (fig. 2 (24)) and second power conductors and a second input port (fig. 2 bus (25) connected to (58)) coupled to the

reference potential, the other of the first and second power conductors coupled directly to the reference potential (fig. 2), the impedance network having coupled between the first and second input ports at least one of a resistive (fig. 2 (100)) or inductive load.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the impedance network of Konrad et al. into the system of Sugishima et al. for the purpose of discharging the voltage on the power conductor whereby stabilizing the system (column 7, lines 32-58).

Referring to claim 18, Sugishima et al. discloses the method as claimed wherein the step of interrupting comprises opening switches within the switching mechanism that selectively couples the motor to the first and second power conductors (column 4, lines 27-66).

7. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Schantz et al.

Referring to claim 6, Sugishima et al. discloses the system as claimed except for a high impedance network having a first terminal coupled to the first power conductor, a second terminal coupled to the second power conductor, and a third terminal coupled to reference potential for equally balancing the voltages developed at the first and second power conductors with respect to the reference potential.

Schantz et al. discloses a system for detecting faults between a power source and a chassis comprising a high impedance network (fig. 6 (109)) having a first terminal coupled to the first power conductor (fig. 6 (+)), a second terminal coupled to the second power conductor (fig. 6 (-)), and a third terminal (fig. 6 (119)) coupled to reference

potential (fig. 6 (115)) for equally balancing the voltages developed at the first and second power conductors with respect to the reference potential.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the high impedance network of Schantz et al. into the system of Sugishima et al. for the purpose of equally splitting the voltage on the first and second power conductors whereby improving stability (column 7, lines 59-67).

8. Claims 8, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Sway-Tin et al.

Referring to claims 8 and 13, Sugishima discloses the system as claimed except for a first capacitor having a first terminal coupled to one of the first and second power conductors, and a second terminal coupled to the reference potential.

Sway-Tin et al. discloses a fault detection system comprising a first capacitor (fig. 2 (C18)) having a first terminal coupled to one of the first (fig. 2 (26)) and second power conductors, and a second terminal coupled to the reference potential (fig. 2).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the capacitor of Sway-Tin et al. into the system of Sugishima et al. for the purpose of smoothing the signal on conductor whereby making data more reliable.

9. Claims 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Dollar, II et al.

Referring to claim 11, Sugishima et al. discloses the system as claimed except wherein said detector is a current sensor having a first port coupled to the first power conductor and a second port coupled to the reference potential via a capacitor.

Dollar, II et al. discloses a fault detection system comprising a current sensor (fig. 2 (20)) having a first port coupled to the first power conductor (fig. 2 (24)) and a second port coupled to the reference potential (fig. 2 (16)) via a capacitor (fig. 2 (60)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the current sensor of Dollar, II et al. into the system of Sugishima et al. for the purpose of additionally filtering the sensed signal whereby providing a more accurate current reading (column 5, line 46 – column 6, line 3).

Referring to claim 12, Sugishima et al. discloses the system as claimed except wherein the processing circuit comprises a capacitor having a first terminal coupled to the first power conductor and a second terminal coupled to a transformer for providing an attenuated signal component relative to the reference potential; and a comparator responsive to the attenuated signal component for comparing with said threshold value for providing said output signal.

Dollar, II et al. discloses a capacitor (fig. 1 (32)) having a first terminal (fig. 1 (26)) coupled to the first power conductor and a second terminal coupled to a transformer (fig. 1 (34)) for providing an attenuated signal component relative to the reference potential; and a comparator (fig. 1 (22)) responsive to the attenuated signal component for comparing with said threshold value for providing said output signal.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the processing circuit of Dollar, II et al. into the system of Sugishima et al. for the purpose of isolating the power conductor from the comparator whereby providing more accurate results (column 4, lines 37-39).

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Sway-Tin et al. as applied to claim 13 above, and further in view of Schantz et al.

Sugishima et al. as modified discloses the system as claimed except for a high impedance network coupled between the first and second power conductors for equally balancing the power distributed from the power distribution unit between a maximum positive voltage and minimum negative voltage with respect to the reference potential.

Schantz et al. discloses a high impedance network (fig. 6 (109)) coupled between the first (fig. 6 (+)) and second (fig. 6 (-)) power conductors for equally balancing the power distributed from the power distribution unit between a maximum positive voltage and minimum negative voltage with respect to the reference potential (fig. 6 (115)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the high impedance network of Schantz et al. into the system of Sugishima et al. as modified for the same purpose as given in claim 6, above.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Sway-Tin et al. as applied to claim 13 above, and further in view of Konrad et al.

Referring to claim 15, Sugishima et al. as modified discloses the system as claimed except wherein the detector comprises an RC filter coupled to the first power conductor for providing an attenuated signal component relative to the reference

potential; and a comparator responsive to the attenuated signal component for comparing with a threshold voltage for providing said control signal.

Konrad et al. discloses an RC filter (column 3, lines 26-29) coupled to the first power conductor for providing an attenuated signal component relative to the reference potential; and a comparator (fig. 2 (90)) responsive to the attenuated signal component for comparing with a threshold voltage for providing said control signal.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the filter of Konrad et al. into the system of Sugishima et al. as modified for the same purpose as given in claim 4, above.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Sway-Tin et al. as applied to claim 13 above, and further in view of Dollar, II et al.

Sugishima et al. as modified discloses the system as claimed except wherein the detector comprises a capacitor having a first terminal coupled to the first power conductor and a second terminal coupled to a transformer for providing an attenuated signal component relative to the reference potential; and a comparator responsive to the attenuated signal component for comparing with said predetermined threshold.

Dollar, II et al. discloses a capacitor (fig. 1 (32)) having a first terminal (fig. 1 (26)) coupled to the first power conductor and a second terminal coupled to a transformer (fig. 1 (34)) for providing an attenuated signal component relative to the reference potential; and a comparator (fig. 1 (22)) responsive to the attenuated signal component for comparing with said predetermined threshold.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the processing circuit of Dollar, II et al. into the system of Sugishima et al. as modified for the same purpose as given in claim 12, above.

13. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Konrad et al. as applied to claim 17 above, and further in view of Suzuki.

Sugishima et al. as modified discloses the method as claimed except wherein the step of sensing the voltage signal on the first power conductor comprises capacitively sensing a square wave voltage signal developed at the first power conductor and having a peak value corresponding to the magnitude of the voltage of the power source.

Suzuki discloses a ground fault detector wherein the step of sensing the voltage signal on the first power conductor comprises capacitively sensing a square wave voltage signal (fig. 3 (c)) developed at the first power conductor and having a peak value (fig. 3 (Va)) corresponding to the magnitude of the voltage of the power source.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the voltage sensor of Suzuki into the method of Sugishima et al. as modified for the purpose of correctly detecting and processing the signal on the conductor whereby providing a more accurate output signal to use for fault determination.

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugishima et al. in view of Konrad et al. as applied to claim 17 above, and further in view of Schantz et al.

Sugishima et al. as modified discloses the method as claimed except for the step of providing a high impedance network between the first and second power conductors

for equally balancing the voltages developed at the first and second power conductors with respect to the reference potential.

Schantz et al. discloses the step of providing a high impedance network (fig. 6 (109)) between the first (fig. 6 (+)) and second (fig. 6 (-)) power conductors for equally balancing the voltages developed at the first and second power conductors with respect to the reference potential (fig. 6 (115)).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the high impedance network of Schantz et al. into the system of Sugishima et al. as modified for the same purpose as given in claim 6, above.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to show the state of the art with respect to ground fault detection.

USPN 6,456,946 to O'Gorman: This patent shows a system for detecting a fault in a motor using a current sensor and a filter.

USPN 5,686,839 to Takagi: This patent shows an electrical leakage detector for an electric vehicle with switches operable to disconnect the motor from the power source.

USPN 5,309,349 to Kwan: This patent shows a current detector for a three-phase AC system wherein current is detected on the first power conductor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is 703-305-7396. The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 703-308-0750. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TJD
June 16, 2003

N. Le
Supervisory Patent Examiner
Technology Center 2800